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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/741,857
Filing Date: December 22, 2000
Appellant(s): MODELSKI ET AL.

Holmes W. Anderson
Reg. No. 37,272
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/16/2009 appealing from the Office action mailed 10/17/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2006/0156303	Hooper et al.	7-2006
7093109	Davis et al.	8-2006
7111156	Mang et al.	9-2006
6813243	Epps et al.	10-2004

6292845 Fleck et al. 09-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim rejections-35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-3 and 5-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1:

The term "specialized" in claims 1 and 5 is a relative term which renders the claims indefinite. The term "specialized" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Without disclosures a standard for ascertaining the requisite degree for the term "specialized"; how would one of ordinary skill in the art determine the claim feature of "selecting a pipeline from a plurality of pipelines, at least some of which are specialized..." The corrections are required.

Regarding claims 2-3 and 5-18:

Those claims are rejected under rationales of claim 1.

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5 and 17 are rejected under 35 U.S.C 103(a) as being un-patentable over Hooper (U.S. 2006/0156303) in view of Davis (U.S. 7,093,109) and further in view of Mang et al. (U.S. 7,111,156).

Regarding claim 1:

Hooper discloses the invention substantially as claimed, including a method, which can be implemented in a computer hardware or software code for routing a data packet, comprising:

producing a plurality of threads associated with the packet: (Hooper discloses a method of producing a number of threads for a data packet wherein each portion of the data packet is processed by different thread(s): abstract; [0003]; [0025]; [0085]).

processing of each packet is divided into multiple independent threads which are processed by multiple pipelines, and such that delay in processing of a first packet routing thread in a first pipeline does not affect processing of a second packet routing thread in a second pipeline: (Hooper discloses method of producing a number of threads for a data packet wherein each portion /or unit of the data packet is processed by each different thread in parallel and independently. It is essential to understand that delay in processing of first portion of packet should not effect processing of other portions of packet if they are processed parallel and independently (abstract, lines 2-6; [0023]; [0032], lines 6-12; [0033-0035]).

assigning a thread identifier (TID) to each of the threads and maintaining an activity status for each thread: (an table maintains number of thread identifiers in association with their activity statuses: Hooper, figure 2; figure 3, items S1, S2, S4; figure 5).

However, Hooper does not explicitly disclose each thread being a sequence of instructions that facilitates packet routing and independently executable with respect to other ones of the threads.

In analogous art, Davis discloses each of threads is process in independent executing a sequence of instructions, see (Davis, column 3, lines 49-51; column 4, lines 5-6, 9-11).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Davis's ideas of process each of threads in independent executing a sequence of instructions into Hooper's system in order to in crease efficiencies for multi-threads processing system, such as, to minimize the impact of latency in data process, see (Davis, column 1, lines 14-17).

However, Hooper-Davis does not explicitly disclose selecting a pipeline from a plurality of pipelines, at least some of which are specialized, and forwarding that thread to the selected pipeline.

In analogous art, Mang discloses a multi-threads processing system, therefrom an application (26) is broken into number of different threads (i.e. thread 28, thread 30, thread 32, thread 34) (see, Mang, figure 7, items 26, 28, 30, 32). Each of the different threads is managed by each of different thread controllers (Mang, figure 7, items 28, 34, 18, 22). The controller manages a corresponding thread and provides operation codes those executed during processing the corresponding thread (see, Mang, column 30, lines 21-28; 47-67; column 28, lines 49-67, 24-

27, 4-15; figure 7; figure 1, figure 2; figure 6). Wherein thread pipeline is forming from combination of operation codes for thread execution and is selected in regarding thread priority, see (column 28, lines 49-67, 24-27, 4-15; figure 7). It clearly shows that the pipeline is designed for a particular purpose (i.e. priority of thread), Therefore the pipeline in Mang's reads on 'specialized pipeline' as claimed.

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Mang's ideas of designing a pipeline for a particular purpose (i.e. priority of thread) into Hooper-Davis's system in order provide an efficient multi-threads communication system with faster process and limited memory requirements, (Mang, column 1, lines 45-49).

Regarding claim 5:

Hooper discloses the invention substantially as claimed, including an apparatus, which can be implemented in a computer hardware or software code for routing a data packet, comprising:

a memory for storing: (Hooper, [0025]).

a plurality of threads associated with the packet: (Hooper discloses method of producing a number of threads for a data packet wherein each portion of the data packet is processed by different thread(s): abstract; [0003]; [0025]; [0085]).

a unique Thread Identifier (TID) for each thread; an activity status for each thread: (an table includes information of thread identifiers in association with activity status for each thread: Hooper, figure 2; figure 3, items S1, S2, S4; figure 5).

processing of each packet is divided into multiple independent threads which are processed by multiple pipelines, and such that delay in processing of a first packet routing thread in a first pipeline does not affect processing of a second packet routing thread in a second pipeline: (Hooper discloses method of producing a number of threads for a data packet wherein each portion or unit of the data packet is processed by each different thread in parallel and independently. It is essential to understand that delay in processing of first portion of packet should not effect processing of other portions of packet if they are processed parallel and independently (abstract, lines 2-6; [0023]; [0032], lines 6-12; [0033-0035]).

However, Hooper does not explicitly disclose each thread being a sequence of instructions that facilitates packet routing and that is independently executable with respect to other ones of the threads.

In analogous art, Davis discloses each of threads is process in independent executing a sequence of instructions, see (Davis, column 3, lines 49-51; column 4, lines 5-6, 9-11).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Davis's ideas of process each of threads in independent executing a sequence of instructions into Hooper's system in order to in crease efficiencies for multiple threads processing system, such as, to minimize the impact of latency in data process, see (Davis, column 1, lines 14-17).

However, Hooper-Davis does not explicitly disclose an analysis machine including a plurality of pipelines, at least some of which are specialized, the analysis machine selecting a pipeline for each thread and forwarding that thread to the selected pipeline.

In analogous art, Mang discloses a multi-threads processing system, therefrom an application (26) is broken into number of different threads (i.e. thread 28, thread 30, thread 32, thread 34) (see, Mang, figure 7, items 26, 28, 30, 32). Each of the different threads is managed by each of different thread controllers (Mang, figure 7, items 28, 34, 18, 22). The controller manages a corresponding thread and provides operation codes those executed during processing the corresponding thread (see, Mang, column 30, lines 21-28; 47-67; column 28, lines 49-67, 24-27, 4-15; figure 7; figure 1, figure 2; figure 6). Wherein thread pipeline is forming from combination of operation codes for thread execution and is selected in regarding thread priority, see (column 28, lines 49-67, 24-27, 4-15; figure 7). It clearly shows that the pipeline is designed for a particular purpose (i.e. priority of thread), Therefore the pipeline in Mang's reads on 'specialized pipeline' as claimed.

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Mang's ideas of designing a pipeline for a particular purpose (i.e. priority of thread) into Hooper-Davis's system in order provide an efficient multi-threads communication system with faster process and limited memory requirements, (Mang, column 1, lines 45-49).

Regarding claim 3:

In addition to rejection in claim 1, Hooper-Davis-Mang further discloses the activity status indicates that a status of the associated thread is one of active, inactive or waiting: (Hooper, figure 2; figure 3, items S1, S2, S4; figure 5).

Regarding claim 17:

In addition to rejection in claim 5, Hooper-Davis-Mang further discloses the activity status indicates that a status of the associated thread is one of active, inactive or waiting: (Hooper, figure 2; figure 3, items S1, S2, S4; figure 5).

Claim 2 is rejected under 35 U.S.C 103(a) as being un-patentable over Hooper-Davis-Mang in view of Epps et al. (U.S. 6,813,243).

Regarding claim 2:

Hooper-Davis-Mang discloses the invention substantially as disclosed in claim 1, but does not explicitly teach steps of transferring the multi-IP packet thread from an input buffer to a packet task manager; dispatching the multi-IP packet thread from the packet task manager to an analysis machine; classifying the multi-IP packet thread in the analysis machine; and modifying and forwarding the multi-IP packet thread in a packet manipulator.

In analogous art, Epps teaches methods for transferring data from an input buffer (Fig 2, item 215) to a packet task manager (Fig 2, items 130, 285, 280; figure 4; column 7, lines 10-44; Column 5, lines 50-55); dispatching the data from the packet task manager to an analysis machine (figure 4; column 7, lines 44-67); classifying the data in the analysis machine (Column 6, lines 33-37); and modifying and forwarding the data in a packet manipulator (figure 4; column 7, lines 44-67); a packet manipulator (Epps, Figure 4, items 450, 460) operationally connected to said analysis machine (Epps, Figure 4).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's those ideas into Hooper-Davis-Mang's system in order to increase efficiencies for data transmission network (e.g. maximum transmission speed), see (Epps: column 3, lines 5-7, lines 40-45).

Claims 6-16 and 18 are rejected under 35 U.S.C 103(a) as being un-patentable over Hooper-Davis-Mang in view of Epps et al. (U.S. 6,813,243) and further in view of Fleck et al. (U.S. 6,292,845).

Regarding claim 6:

Hooper-Davis-Mang discloses the invention substantially as disclosed in claim 5, but does not explicitly teach a packet manager operatively connected to analysis machine; and packet manipulator operationally connected to said analysis machine.

In analogous art, Epps discloses a packet task manager (Epps, Figure 2, item 130, Column 5, lines 50-55) operationally connected to said analysis machine (Epps, Figure 2; Column 6, lines 33-37); a packet manipulator (Epps, Figure 4, items 450, 460) operationally connected to said analysis machine (Epps, figure 3; fig 4, column 15, lines 32-67; column 7, lines 12-67; column 8, lines 1-67; column 9, lines 1-67; column 10, lines 1-67).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's those ideas into Hooper-Davis-Mang's system in order to increase efficiencies for data transmission network (e.g. maximum transmission speed), see (Epps: column 3, lines 5-7, lines 40-45).

However, Hooper-Davis-Mang - Epps does not explicitly disclose a machine having multiple pipelines; wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field.

In analogous art, Fleck's system including multiple pipelines: (column 3, lines 61-67; column 4, lines 1-67; column 5, lines 59-62; column 6, lines 7-34).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Fleck's ideas of including multiple pipelines into Hooper-Davis-Mang - Epps's system in order to increase efficiencies for data transmission system, see (Fleck: column 3, lines 61-67).

Regarding claim 7:

In addition to rejection in claim 6, Hooper-Davis-Mang - Epps- Fleck further discloses the activity status indicates one of active, inactive or waiting: (Hooper, figure 2; figure 3, items S1, S2, S4; figure 5).

Regarding claim 8:

In addition to rejection in claim 6, Hooper-Davis-Mang - Epps- Fleck further discloses 32 threads, although Hooper-Davis-Mang - Epps- Fleck does not specifically disclose analysis machine has 32 threads, such limitations are merely a matter of design choice and would have been obvious in system of Hooper-Davis-Mang - Epps- Fleck.

Regarding claim 9:

In addition to rejection in claim 6, Hooper-Davis-Mang - Epps- Fleck further discloses a packet task manager (Epps, Figure 2, item 130; Column 5, lines 50-55) operationally connected to said analysis machine (Epps, Figure 2; Column 6, lines 33-37); a packet manipulator (Epps, Figure 4, item 450, 460) operationally connected to said analysis machine (Epps, Figure 4); a global access bus including a master request bus (Epps, Figure 4, item 496) and a slave request bus (Epps, Figure 4, item 497) separated from each other and pipelined (Epps, Figure 4, items 410-460).

Regarding claim 10:

In addition to rejection in claim 6, Hooper-Davis-Mang - Epps- Fleck further discloses an external memory engine (Figure 4, item 215) operationally connected to said analysis machine (Epps, Figure 4, item 420; Column 6, lines 30-35) wherein the analysis machine classifies packet data; a hash engine (Epps, Figure. 4, item 430; Column 24, lines 24-28) operationally connected to said analysis machine (Epps, Column 24, lines 24-48).

Regarding claim 18:

In addition to rejection in claim 9, Hooper-Davis-Mang - Epps- Fleck further discloses a bi-directional access port operationally connected to said analysis machine (Epps, Column 25, lines 1-7, wherein the input/output port are PPP/HDLC); an input buffer (Epps, Figure 2, item 215) operationally connected to said analysis machine (input buffer operationally connected to Prep Stage: Figure 4, item 420 / analysis machine through the pipeline); and an output buffer (Epps, Fig 2, item 1430) operationally connected to said analysis machine (transmit FIFO operationally connected to Prep Stage Figure 4, item 420 through the switch fabric).

Regarding claim 11:

In addition to rejection in claim 9, Hooper-Davis-Mang - Epps- Fleck further discloses packet input global access bus program code, stored in a computer readable memory and operable when executed to control a flow of data packet information from a flexible input data buffer to the analysis machine (Epps: Column 4 44, lines 60-67; Column 45, lines 1-15).

Regarding claim 12:

In addition to rejection in claim 9, Hooper-Davis-Mang - Epps- Fleck further discloses packet data global access bus program code, stored in a computer readable memory and operable when executed to control a flow of packet data between a flexible data input bus and the packet

manipulator: (Mang, column 3, lines 63-67; column 4, lines 1-8, column 10, lines 32-37; column 11, lines 1-14).

Regarding claim 13:

In addition to rejection in claim 9, Hooper-Davis-Mang - Epps- Fleck further discloses statistics data global access bus software code used for connection of the analysis machine to the packet manipulator: (Mang, column 3, lines 63-67; column 4, lines 1-8, column 10, lines 32-37; column 11, lines 1-14).

Regarding claim14:

In addition to rejection in claim 9, Hooper-Davis-Mang - Epps- Fleck further discloses private data global access bus software code used for connection of the analysis machine to an internal memory engine sub-module: (Mang, column 3, lines 63-67; column 4, lines 1-8, column 10, lines 32-37; column 11, lines 1-14).

Regarding claim 15:

In addition to rejection in claim 9, Hooper-Davis-Mang - Epps- Fleck further discloses lookup global access bus software code used for connection of the analysis machine to an internal memory engine sub-module: (Mang, column 3, lines 63-67; column 4, lines 1-8, column 10, lines 32-37; column 11, lines 1-14).

Regarding claim 16

In addition to rejection in claim 9, Hooper-Davis-Mang - Epps- Fleck further discloses results global access bus software code used for providing flexible access to an external memory: (Mang, column 3, lines 63-67; column 4, lines 1-8, column 10, lines 32-37; column 11, lines 1-14).

(10) Response to Argument:

a) Appellant argues to claims 1 and 5 with respect to:

The Office Action did not consider claim limitation "delay in processing of a first packet routing thread in a first pipeline does not affect processing of a second packet routing thread in a second pipeline."

In reply to Appellant's arguments:

This limitation was addressed in the Office action (see page 3, lines 20-23), and the limitation was rejected under light of Hooper (U.S. 2006/0156303).

Hooper discloses a similar multi-threads processor system (Hooper, [0022]). In Hooper's system, a packet could be broken down into number of portions (Hooper, [0026], lines 16-21). Each of the portions of data packet is processed by the processor under different threads in parallel and independently (Hooper, [0023], lines 6-11; [0026], lines 16-21; [0032], lines 6-12; [0083]; [0085], lines 1-5). It is essential to understand that delay in processing of first portion of packet should not effect processing of other portions of packet if they are processed parallel and independently (Hooper, abstract, lines 2-6; [0023]; [0032], lines 6-12; [0033-0035]).

b) Appellant argues to claims 1 and 5, with respect to:

"The Examiner concedes that Hooper fails to disclose **producing a plurality of threads associated with the packet** where each thread is a sequence of instructions that facilitates packet routing and that is independently executable with respect to each other ones of the

threads. However, the Examiner asserts that the feature is taught by Davis…" (see Appeal Brief, page 8, lines 17-20).

In reply to Appellant's arguments:

In the Office Action, Examiner did not admit that Hooper fails to disclose feature of "**producing a plurality of threads associated with the packet,**" (see, the Office Action, page 4, lines 4-6). And also Examiner did not assert that this limitation is taught by Davis.

In fact, in the Office Action, the limitation of "**producing a plurality of threads associated with the packet**" was rejected under light of Hooper (U.S. 2006/0156303) (see, the Office Action, page 3, lines 17-19). Hooper teaches that a packet could be broken down into number of portions (Hooper, [0026], lines 16-21). Each of the portions of data packet is processed by the processor under different threads in parallel and independently (Hooper, [0026], lines 16-21; [0032], lines 6-12).

Originally, in the Office Action, Examiner only conceded that the claim feature of "each thread being a sequence of instructions that facilitates packet routing and independently executable with respect to other ones of the threads" is not supported by Hooper (see, the Office Action, page 4, lines 4-6). However this limitation is taught by Davis. Such as, Davis teaches plurality of independent instructions execution threads. Those instruction execution threads are queued and independently executable with regard to thread priority, see (Davis, abstract, lines 4-17; figure 3; figure 4; column 4, lines 9-15: *Each of the execution threads is an independent process executing a sequence of instructions as the threads are allowed to gain access to the processor hardware. An additional aspect of the current invention is that the tree search coprocessor is pipelined to enable multiple execution threads to each have access simultaneously*

but at different phases (overlapping) in the tree search pipeline; column 2, lines 17-67; column7, lines 22-35; column 8, lines 10-16; column 6, lines 23-56).

c) Appellant argues to claims 1 and 5, with respect to:

Davids does not disclose "threads are being **independently executable**", but merely "independent."

In reply to Appellant's arguments:

This feature is clearly taught by both Davis and Hooper.

Hooper teaches each portion of data packet is processed by a thread which is executed (Hooper, [0028], lines 17-24; [0029], lines 3-4) in parallel and independently with other threads (Hooper, [0032], lines6-12; [0023], lines 6-11; figure 15).

Davis teaches plurality of independent instruction execution threads. Those are queued and independently executable regarding thread priority, see (Davis, abstract, lines 4-17; figure 3; figure 4; column 4, lines 9-15: *Each of the execution threads is an independent process executing a sequence of instructions as the threads are allowed to gain access to the processor hardware. An additional aspect of the current invention is that the tree search coprocessor is pipelined to enable multiple execution threads to each have access simultaneously but at different phases (overlapping) in the tree search pipeline*; column 2, lines 17-67; column7, lines 22-35; column 8, lines 10-16; column 6, lines 23-56).

d) Appellant argues to claims 1 and 5 with respect to the rejection for claim feature of "specialized pipeline" under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter.

Appellant argues that the term "specialized" is not indefinite because it is understood in the art and described detail in the specification. Appellant defines the term "specialized" which is "unspecialized" by referring to the Merriam-Webster Dictionary. And then Appellant concludes that "the specialized pipeline" is not general, but rather designed for a particular purpose by referring to the citation (page 12, lines 5-12) which included in the specification.

In reply to Appellant's arguments:

Although the appellant's citation, from the specification, does contain the phase "specialized processing pipeline". However, nowhere in the citation discloses the use of designing a pipeline for a particular purpose as admitted by appellant. Because the specification fails to provide a standard for ascertaining the requisite degree for the claim limitation "specialized pipeline", and also the definition of the term "specialized", from Merriam-Webster Dictionary, does not provide a standard for ascertaining the requisite degree for the term "specialized", so that Appellant's arguments are not persuasive and the rejection for claim limitation "specialized pipeline" under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter is retained.

e) Appellant argues to claims 1 and 5 with respect to:

Mang does not disclose feature of 'specialized pipeline'.

In reply to Appellant's arguments:

This feature is clearly taught by Mang. Particularly, Mang discloses a multi-threads processing system, therefrom an application (26) is broken into number of different threads (i.e. thread 28, thread 30, thread 32, thread 34) (see, Mang, figure 7, items 26, 28, 30, 32). Each of the different threads is managed by each of different thread controllers (Mang, figure 7, items 28, 34, 18, 22). The controller manages a corresponding thread and provides operation codes those are executed during processing the corresponding thread (see, Mang, column 30, lines 21-28; 47-67; column 28, lines 49-67, 24-27, 4-15; figure 7; figure 1, figure 2; figure 6). Thread pipeline is forming from combination of operation codes those are selected to be filled into the thread pipeline with regard to thread priority, see (Mang, column 28, lines 49-67, 24-27, 4-15; figure 7). Consequently, it clearly shows that the thread pipeline is designed for a particular purpose (i.e. priority of thread), therefore the thread pipeline in Mang's reads on 'specialized pipeline' as claimed by appellant.

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

/Lan-Dai Truong/
Patent Examiner.
06/04/2009

Conferees:

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